PCI Express testing using the DTG5000 Data Timing Generator

▶ With the integration of PCI Express into all future PCs, the requirement for interoperability is essential to guarantee it's success. Compliance testing and characterization tools, such as the DTG5000 Series, help to solve these testing needs.

INTRODUCTION

With digital data becoming part of every piece of our communication exchange, the requirement for changing the PC architecture from the existing wide parallel bus (PCI) structure to a much faster serial data transmission method (PCI Express) is finally being realized. In order to test these new devices such as receivers, Serializer/De-serializer (Ser-Des), cables and connectors specific test methods and equipment is required. This note discusses how to setup and use the Tektronix DTG5000 Series Data Timing Generator for specific design and verification testing of PCI Express devices.

PCI Express Overview

PCI Express, formally known as 3GIO (Third Generation I/O) is the direct replacement for the existing PCI bus. It uses Low Voltage Differential Signaling (LVDS), a packet-based data transmission protocol, and an extendable high-speed data rate beginning at 2.5 Gb/s or an individual pin rate of 100M bit/sec and future expansions up to 4X. It uses a 4-wire interface to provide a bi-directional transmit signal pair and receive signal pair on each serial data lane. It also defines the capability of aggregating lanes up to a width of 32 lanes, depending on the application and adding 3.5dB of de-emphasis to transition events to compensate for ISI (Inner Symbol Interference) and interconnect losses. Although more wires are required per data bit than with a conventional data bus, the message-based protocol and embedded clocking eliminates the need for the many data control signals required by a conventional data bus. The elimination of data transfer control signals in the interface results in no major increase in the size of backplane connectors, even with 4 wires per bit for bi-directional differential signaling. The data rate includes a 20% overhead for 8B/10B encoding. This data encoding provides a DC-balanced bit stream with high transition density and also provides special control characters for the data transfer protocol. The DC-balanced bit stream allows for AC-coupling and improved signal integrity, and the high transition density eases the task of clock recovery at the SERDES receiver which integrates the parallel-to-serial and serial-to-parallel functions into a common building block component for high speed serial transmission and also the re-use of existing link layer components. It will be used to connect storage and

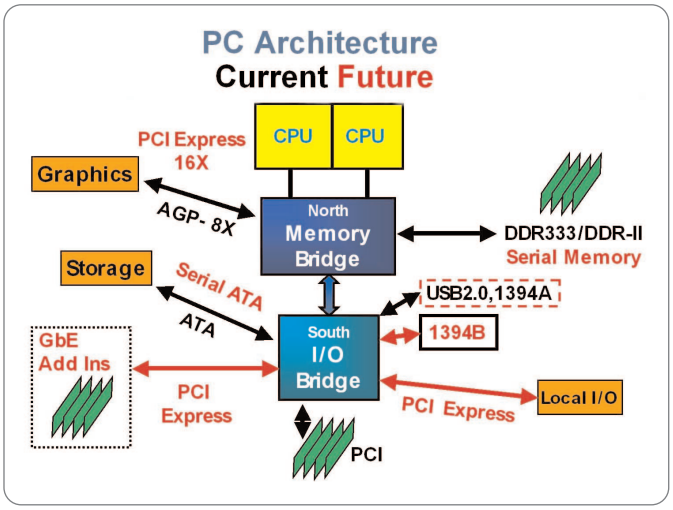
network devices to a server and replaces the current PC architecture in which the memory attaches to the North Bridge in the processor. In PCI Express, the memory still attaches to the processors' North Bridge, but that in turn connects to the PCI Express bus and eliminates proprietary components. Either the PCI-X or PCI Express buses attach from I/O bridge to the fabric interconnect, whether it is InfiniBand, Ethernet, or other add-in devices.

PCI Express Physical Layer Receiver Testing Overview

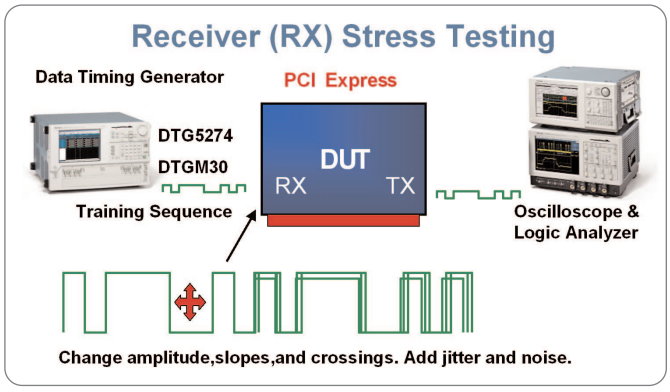
The PCI Express base specification was developed to guarantee interoperability between many manufacturers by a consortium of companies called PCI SIG and is available through membership at www.pcisig.com. Within this specification all the definitions and testing requirements can be found. In any PCI Express device there will be a Transmitter (TX) section and a Receiver (RX) section. For this particular note we will be discussing tests required in the RX physical layer specifications found in section 4 of the base specification.

To validate engineering designs and manufacturing process of PCI Express receiver components, specific tests and equipment are recommended. For receiver testing a stimulus device is required. This stimulus or Timing Generator in this case must have the capability of generating specific 2.5Gb/s test patterns such as a Training Sequence (TS1 & TS2) to the device. If this training sequence is recognized within the device's receiver, a similar sequence is outputted from the transmitter section and then can be validated with an oscilloscope and/or a Logic Analyzer. In order to guarantee interoperability, this training pattern can be sent normally or altered such that the device under test's (DUT's) performance can be characterized. These alterations need to be able to stress the device in various ways. Specific tests would include eye-diagram, mask testing, amplitude level variations; eye-crossing level changes, differential skew variances, as well as jitter analysis with RJ, DJ and Tj and added noise.

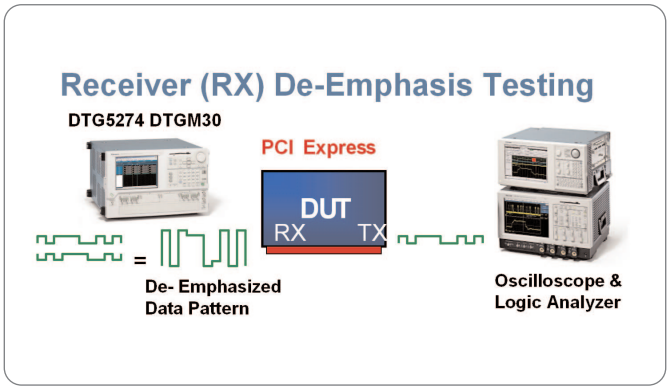
Also, when testing receivers there is the requirement for the Data Timing Generator to send de-emphasized bits on consecutive transition bits to test the SerDes circuits of the DUT.



▶ ***Figure 1.*** *PC current and future architecture.*



▶ ***Figure 2.*** *Rx testing.*



▶ ***Figure 3.*** *Rx de-emphasis.*

PCI Express Physical Layer Receiver Testing Detail

Here we see a diagram showing some of the electrical specifications and requirements for testing. We also see the requirement to test for variances in amplitudes, and also minimum eye width, this is usually caused by random and deterministic jitter.

The first requirement for RX testing is the ability to send the Training Sequence to the device. This training sequence or TS1 and TS2 can be loaded into the DTG5274 as a setup or it can be imported into the DTG using several different ASCII formats. These sequences are composed of ordered sets used for bit alignment, symbol alignment and to exchange physical layer parameters. Training sequence ordered sets are never scrambled but are always 8b/10b encoded. TS1 and TS2 tables can be found in Table 4-2 and 4-3 of the PCI Express base specification rev 1.0a. Once the nominal TS1 and TS2 sequences are sent to the DUT RX input verification and performance can be monitored at the TX side of the device using the Oscilloscope and Logic Analyzer. Once it has been verified that the device works with nominal values, then alterations can be made to the sequence to stress the device and find the limits of it's performance. We will explore some of these tests.

The DTG5000 Series with it's Windows ™ interface allows the user to easily modify key parameters of the pattern. By selecting the Level icon, one can adjust min and max levels and also enter limits to guarantee that levels don't exceed device tolerances. The DTG5000 Series recommended configuration for PCI Express testing would be a DTG5274 in conjunction with the DTGM30 output module. This configuration has differential outputs and supports up to 8 differential channels and several receivers could be tested with one setup. Besides amplitude levels, other characteristics of the data can be altered to test performance levels of the DUT. Examples of other tests include:

– Timing tolerances (varying the frequency and delays to find the RX limits).
  – Using the easy to use Timing menu, adjustments to frequency and delays between channels and groups can be adjusted. These delays can be used to simulate skew as small as .2ps between data lines and multiple lanes can be used when testing devices that have X2, X4, X8 and X16 lanes of RX traffic.
  – Delay between differential pairs (simulates differential skew between each differential pair). This can be used to simulate board layout delays that may effect circuit performance.
– Crossing level tolerances. (The DTG5000 Series allows you to vary the crossing point from 30% to 70% of the high low amplitude)
– Jitter and noise generation.

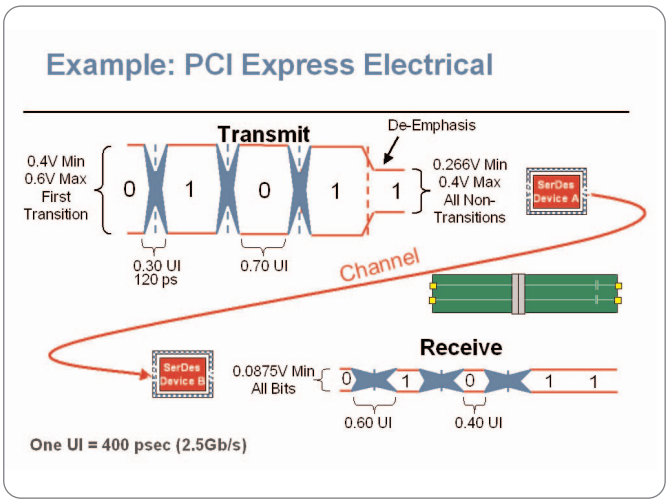


Figure 4. *PCI Express Electrical Specifications.*

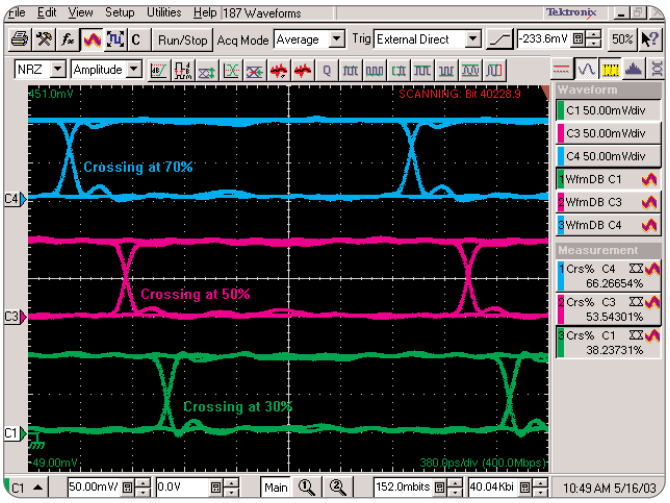
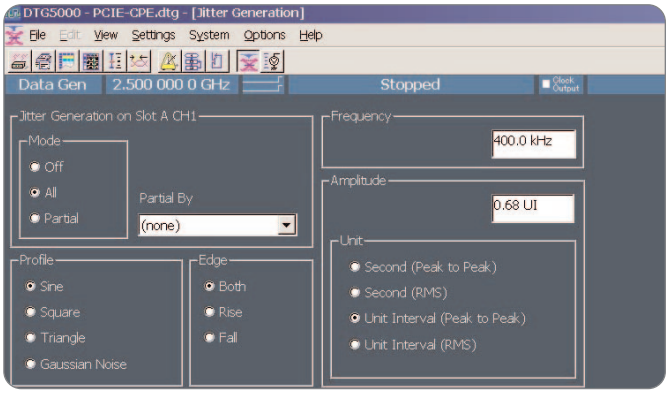


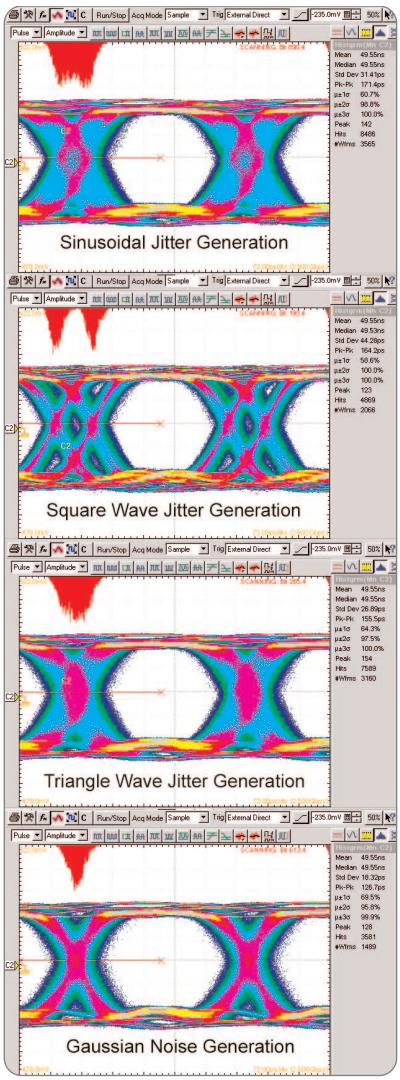
Figure 5. *Crossing level variances.*

The DTG5000 Series has a built in jitter and noise generator to stress devices to specific requirements (Figure 6). This jitter generator can use different profiles such as sine, square, triangle and noise.

Figures 7 shows the different types of jitter applied using the built in jitter generator. A histogram shows the different jitter distributions depending on the profile used. Notice that the square wave profile is more of a deterministic type where sine or triangle could be used to generate more of a random jitter effect. The jitter generator also provides the ability to generate jitter on the rising or falling edges or both. The max freq is limited to 1.56MHz but this is enough to stress most devices enough to characterize them sufficiently. The PCI Express Base Specification Rev 1.0a Table 4.3.4 specifies jitter as the measurement variation of the crossing points in relation to a recovered TX UI. The DTG5000 Series allows you to control how much jitter you apply in UI amplitude and using specific frequency content. Because this jitter generation is built into the DTG Series, there is no need for an external source. This reduces the test setup and makes overall test time shorter. With the versatility of the DTG Series, not only compliance testing can be done but characterization of devices can also be accomplished. Using jitter generation to examine effects caused by jitter and noise components by simulating random or deterministic jitter is a valuable tool in device design. With 400kHz frequency content the jitter amplitude can be as high as .68 UI which is within the specification required to stress the receiver to see if meets the maximum jitter specified.



▶ ***Figure 6.*** *DTG5000 Jitter/Noise generator menu.*



▶ ***Figure 7.*** *Types of jitter generation.*

Also part of the receiver testing is the requirement for the Data Timing Generator to simulate de-emphasis patterns.

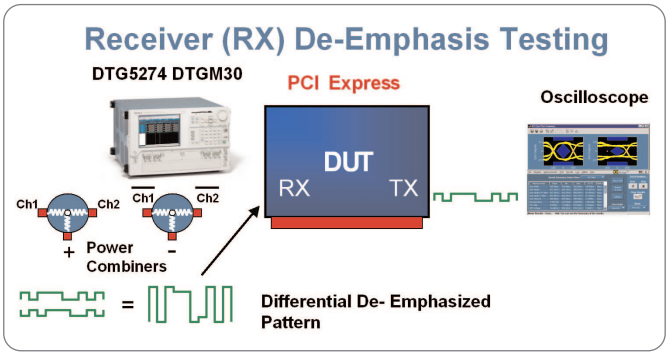
De-emphasis must be implemented when multiple bits of the same polarity are output in succession. Subsequent bits are driven at a differential voltage level 3.5 dB (+/-.5 dB) below the first bit. Note that individual bits, and the first bit from a sequence in which all bits have the same polarity, must always be driven between the Min and Max values as specified by VTX-DIFFp-p in Table 4-5 of the PCI Express Base specification.

In order to generate these de-emphasis patterns special techniques need to applied. These techniques incorporate the use of power combiners as part of the setup.

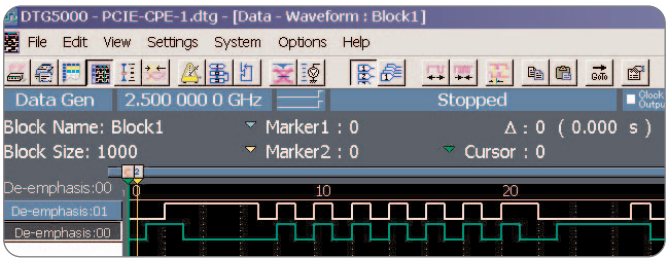
This setup requires loading the de-emphasized pattern in the DTG5274.

Or by loading the PCI Express test pattern into ch1 and then through the DTG waveform menu, copy and paste this into ch2. Once you have the same pattern in both channels, use the timing menu to invert ch2 and delay the clock by one UI or 400ps.

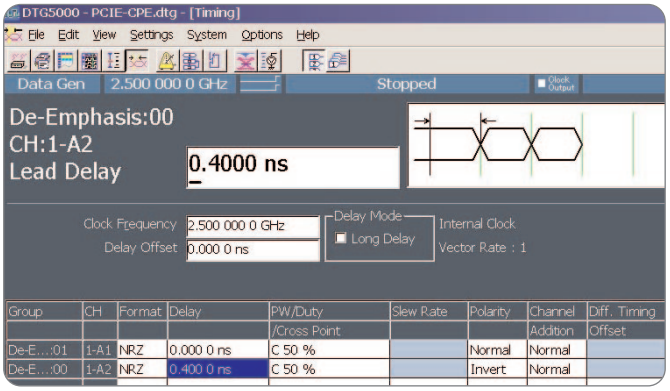
Then by connecting a power combiner from the DTGM30's ch1 and ch2 and another power combiner to the complementary channels of ch1 and ch2 you result in the differential de-emphasized pattern required for RX stress testing into a receiver's Ser-Des device. The amplitude levels will have to adjusted depending on losses incurred in the power combiners (usually 50%) and how much de-emphasis you want to apply.



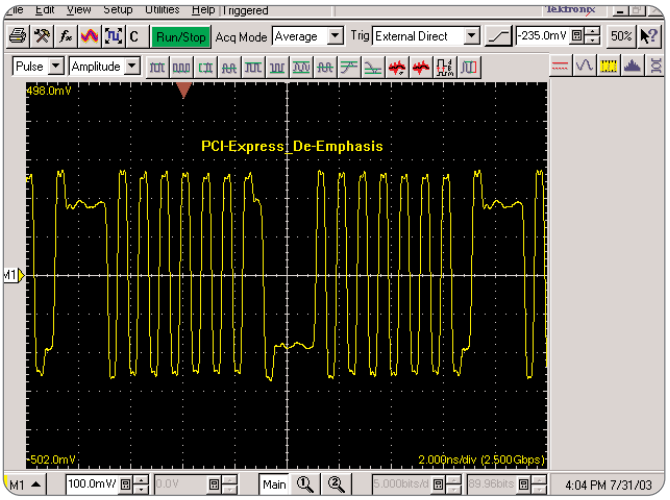
▶ ***Figure 8.*** *De-Emphasis diagram.*



▶ ***Figure 9.*** *DTG5000 Waveform menu.*



▶ ***Figure 10.*** *DTG5000 Timing menu.*



▶ ***Figure 11.*** *De-Emphasis displayed on an Oscilloscope.*

SUMMARY

Because PCI Express solves many of the bottlenecks in current PC architecture. Designers of PC related devices are hot to get these devices developed and in the hands of consumers. In order to guarantee interoperability between many manufacturer's, specific test are required. The DTG5000 Series is a perfect instrument to aid in this testing, especially in the receiver end of the devices.

Tektronix comprehensive, integrated tool set - signal sources, oscilloscopes, logic analyzers, probes and software - enables designers to resolve these issues quickly and efficiently so that they can easily implement PCI-Express into their designs.

Here is a list of instruments Tektronix offers to enable your PCI Express testing:

– DTG5274 and DTGM30 for PCI Express differential serial data pattern stimulation and receiver validation.

– Tektronix TDS6604 or TDS7000 Real time oscilloscope.

For PCI Express, the fundamental signaling frequency is 1.25GHz (half the bit rate) and the minimum specified 20-80 rise-time is 50ps. The TDS6604 Real-Time Digital Storage Oscilloscope provides an analog bandwidth of 6GHz (a 4.8X multiplier on the fundamental frequency) and a 10-90% rise-time of 70ps. This equates to a 20-80% rise time of approximately 50ps.

– TDS RT-Eye Serial Data Compliance and Analysis (Opt. RTE) application, a software tool that operates with Tektronix TDS6000 Series and TDS/CSA7000 Series (1.5GHz and above) oscilloscopes. It provides the features required by customers performing validation and compliance tests on high speed serial buses up to 3.2Gb/s.

– TLA700 Series logic analyzer with TMS817/818 PCI Express Bus Support

The TMS817/818 support packages provide an interface between a PCI Express link and the TLA700 Series logic analyzer so you can use the power of the TLA700 to validate and debug your PCI Express-based design.

– TDS8000B Sampling Oscilloscope with TDR

As with all high speed signaling, board layout and interconnect characterization is critical to good signal integrity. Low Voltage Differential Signaling (LVDS) at 2.5Gb/s over low cost media such as FR4, will pose many layout challenges. The TDS/CSA8000 Series Oscilloscope with the 80E04 sampling head provides true-differential TDR measurements necessary for understanding the transmission characteristics of each differential lane in PCI Express.

Other useful equipment:

– AWG620 and AWG710

Provides the ability to generate serial bit streams of any pattern at bit rates up to 2.6Gb/s. These streams are created using the "marker" outputs of the signal source. Using both marker outputs "MARKER 1" and "MARKER 2" (both driven differentially), a "PCI Express" signal can be produced.

– P7350 or P7350SMA Differential Active Probe.

For analog signal integrity testing, it is assumed by the specification that the link will be broken and terminated into a 100Ω differential (50Ω/side) load. When the transmit SerDes driver sends out a training sequence and does not receive a response, the device concludes that it is transmitting to a piece of test equipment and transmits a repeating compliance test pattern.

Given the architecture, three different probing strategies are recommended for driver (or transmitter) testing.

The first option is to use two TekConnect™ TCA-SMA adapters (one on Ch1 and one on Ch3) of the TDS6604. The differential signal is defined by the math waveform (Ch1-Ch3). This is known as pseudo-differential acquisition. The advantage of this technique is that it takes full advantage of the bandwidth of the oscilloscope. The disadvantage is that the two channels must be de-skewed each time you set up the measurement to insure accurate timing measurements.

The second option is to provide a "dummy" load in a termination block and use the P7350 Differential Active Probe. Since this is a differential probe, channel de-skew is not required.

The final option is to use the P7350SMA probe. The P7350SMA provides a differential SMA input and uses the 5GHz active probing technology in the P7350 to achieve a single channel measurement. The usage and a simplified circuit diagram is shown in Figure 12. The P7350SMA eliminates the need for channel deskew and provides a true differential measurement.

▶ ***Figure 12.*** *Probing PCI Express solutions.*

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